REMARKS/ARGUMENTS

Currently in the case, claims 1-25 were rejected. After amendment, claims 2, 3, 7, 8, 9 and 19 have been cancelled leaving claims 1, 4-6, 10-18, and 20-25 as pending and rejected. The claims and one paragraph of the specification is amended for clarity.

This Amendment responds to the aforementioned Office Action, wherein the claims as originally presented were rejected under Title 35 of United States Code, §§112, 102 & 103. The Examiner's remarks have been carefully considered and, in view of the cited art, the claims which have amended to more particularly point out the distinctly claimed what Applicants regard as the subject matter of this present invention, it is sincerely believed that the claims which remain in the instant case patentably distinguish over all the prior art references. It is respectfully requested that this Application be re-examined in view of the following remarks, that the rejections be withdrawn, and that allowable subject matter be identified.

The points raised by the Examiner in the written office action will be responded to in the order they were discussed by the Examiner in the Office Action.

The invention title has been amended and it is hoped that it will be acceptable to the Examiner. A formal proposed drawing paper is submitted.

Novelty

The Examiner rejected claims 1-19 and 24 as anticipated by U.S. Patent No. 5,784,532 to McDonough.

Amended claim 1 is novel over US Patent 5,926,786 (McDonough) by virtue of the following features. McDonough does not disclose an accelerator core including:

A vector processor which is:
capable of processing multiple items of data simultaneously;
comprises a plurality of similar operational units capable of carrying out simultaneous data processing operations;
and is operative to execute program instructions;
whereby a data processing operation is assigned for performance by one or more of the operational units on a plurality of data elements.

Rather, McDonough discloses a digital signal processor (4) and a minimisation processor (6) in which the minimisation processor comprises dedicated hardware (see Figures 6a, 6b and 15) for performing one of two specific computational operations depending on the setting of a control signal (Figure 15). In one mode of operation (referred to as the minimisation mode), the minimisation processor (6) performs specific mean squared error (MSE) functions and, in a second mode of operation (referred to as the FIR filter mode) the minimisation processor (6) performs specific filter operations (see for example column 42, lines 24 to 56). This is in contrast to the codec of Claim 1 in which the

accelerator core, given that it comprises a vector processor that is operative to execute program instructions, is not a dedicated resource and is not specifically configured to perform specific tasks. It is respectively submitted therefore that Claim 1 is novel under 35 USC 102 (b) when compared to McDonough.

Obviousness

The Examiner rejected claims 20-22 and 24 under 35 U.S.C. § 103 over McDonough in view of U.S. Patent No. 6,314,393 to Yue-Peng Zheng.

The Examiner rejected claim 23 under 35 U.S.C. § 103 over McDonough in view of Zheng, and further in view of U.S. Patent No. 4,926,482 to Frost. The Examiner also rejected claim 25 as unpatentable over McDonough as applied to the rejection of claim 24.

Generally, the object of the McDonough invention is to increase the efficiency in the performance of the vocoding algorithm using a specialised DSP core hardware. The particular aim is to perform the vocoder algorithm in a reduced number of clock cycles and with reduced power consumption (McDonough US 5,926,786) in particular column 2, line 62 to column 3, line 56).

Accordingly, McDonough provides the minimisation processor (6) in order to perform certain specific computations which can be curtailed under certain conditions thereby saving clock cycles

and power consumption (see in particular column 3, lines 30 to 46). These technical aims of McDonough are incompatible with the codec of Claim 1 since the provision of a vector processor as set out in Claim 1 does not allow certain processing operations to be curtailed under certain conditions thereby saving clock cycles.

Moreover, even though McDonough identifies in Table 1 of column 2 of McDonough that the pitch search and the code book search together consume over 75% of the processing time, McDonough still does not chose to perform these operations in an accelerator core. Rather, McDonough's minimization processor (6) performs only those parts of the pitch search and code book search that are susceptible to being curtailed under certain conditions.

Accordingly, it is respectfully submitted that McDonough does not disclose or suggest the novel features of Claim 1 as set out above. Moreover, the teaching of McDonough is technically incompatible with the codec set out in Claim 1 and, as such, McDonough provides no incentive for a skilled person to arrive at the codec in Claim 1. Rather, it is submitted that McDonough would lead the skilled person away from the codec as claimed in Claim 1.

It is further submitted that neither United States Patent 6,314,393 (Zheng) or United States Patent 4,926,482 (Frost) disclose or suggest a codec having an accelerator core with vector processor as set out in Claim 1.

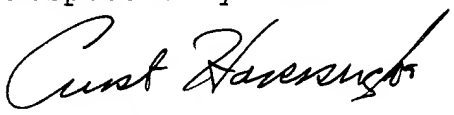
It is respectfully submitted therefore that New Claim 1 is not obvious in the light of McDonough when taken alone or combined with Zheng and or Frost.

Applicant requests reconsideration and ultimate allowability of all aspects of the case, including all of claims 1, 4-6, 10-18, and 20-25.

The Examiner is invited to telephone Applicant's Attorney at the number below between the hours of 1:00 p.m. and 6:00 p.m. Eastern Standard Time, if such will advance this case.

Dated: January 22, 2004

Respectfully submitted:



Curt Harrington
Registration Number 31,456
Suite 250
6300 State University Drive
Long Beach, CA 90815

Tel. (562) 594-9784
Fax.(562) 594-4414
Docket: KELLY-4

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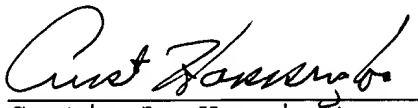

Curtis L. Harrington, Reg. No. 31,456